

One Stop for All Study Materials

& Lab Programs



By K B Hemanth Raj

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| | MPUTER ORGA | | | |
|--|--------------------------|-------------------------------|-----------|---------|
| (Effective | | c year 2018 -2019) | | |
| Course Code | SEMESTER - 18CS34 | - 111 CIE Marks | 40 | |
| Number of Contact Hours/Week | 3:0:0 | SEE Marks | 60 | |
| Total Number of Contact Hours | 40 | Exam Hours | 03 | |
| Total Number of Contact Hours | CREDITS - | | 05 | |
| Course Learning Objectives: This cou | | | | |
| • Explain the basic sub systems o | | | operation | ۱. |
| Illustrate the concept of program | - | - | peration | |
| Demonstrate different ways of contract of the second second | - | | O interf | faces. |
| Describe memory hierarchy and | • | | 0 111011 | |
| Describe arithmetic and logical | • | • | ands | |
| Illustrate organization of a simp | • | e ei i | | systems |
| Module 1 | ie processor, piper | ined processor and other con | ipating | Contact |
| | | | | Hours |
| Basic Structure of Computers: Basic | Operational Conce | epts, Bus Structures, Perform | ance – | 08 |
| Processor Clock, Basic Performance Equation, Clock Rate, Performance Measurement. | | | | |
| Machine Instructions and Program | ms: Memory Lo | ocation and Addresses, M | lemory | |
| Operations, Instructions and Instruct | ction Sequencing, | Addressing Modes, Ass | sembly | |
| Language, Basic Input and Output Ope | | d Queues, Subroutines, Add | litional | |
| Instructions, Encoding of Machine Instr | | | | |
| Text book 1: Chapter1 – 1.3, 1.4, 1.6 (| (1.6.1-1.6.4, 1.6.7), | , Chapter2 – 2.2 to 2.10 | | |
| RBT: L1, L2, L3 | | | | |
| Module 2 | | | | |
| Input/Output Organization: Accessing I/O Devices, Interrupts – Interrupt Hardware, Direct | | | | 08 |
| Memory Access, Buses, Interface Circuits, Standard I/O Interfaces – PCI Bus, SCSI Bus, | | | | |
| USB. | | | | |
| Text book 1: Chapter4 – 4.1, 4.2, 4.4, | 4.5, 4.6, 4.7 | | | |
| RBT: L1, L2, L3 Module 3 | | | | |
| | miconductor RAM | Memories Read Only Mer | nories | 08 |
| Memory System: Basic Concepts, Semiconductor RAM Memories, Read Only Memories, Speed, Size, and Cost, Cache Memories – Mapping Functions, Replacement Algorithms, | | | | 00 |
| Performance Considerations. | | | | |
| Text book 1: Chapter5 – 5.1 to 5.4, 5.4 | 5 (5.5.1, 5.5.2), 5.6 | | | |
| RBT: L1, L2, L3 | | | | |
| Module 4 | | | | |
| Arithmetic: Numbers, Arithmetic Oper | rations and Chara | cters, Addition and Subtract | tion of | 08 |
| Signed Numbers, Design of Fast Adders, Multiplication of Positive Numbers, Signed | | | | |
| Operand Multiplication, Fast Multiplica | | | U | |
| Text book 1: Chapter2-2.1, Chapter6 | – 6.1 to 6.6 | | | |
| RBT: L1, L2, L3 | | | | |
| Module 5 | | | | |
| Basic Processing Unit: Some Fundam | ental Concepts, Ex | ecution of a Complete Instr | uction, | 08 |
| Multiple Bus Organization, Hard-wired | | ogrammed Control. | | |
| Pipelining: Basic concepts of pipelining | - | | | |
| Text book 1: Chapter7, Chapter8 – 8. | .1 | | | |
| RBT: L1, L2, L3 | | | | |
| Course Outcomes: The student will be | | | | |
| Explain the basic organization of the b | of a computer syste | em. | | |

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- Demonstrate functioning of different sub systems, such as processor, Input/output, and memory.
- Illustrate hardwired control and micro programmed control, pipelining, embedded and other computing systems.
- Design and analyse simple arithmetic and logical units.

Question Paper Pattern:

- The question paper will have ten questions.
- Each full Question consisting of 20 marks
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.
- The students will have to answer 5 full questions, selecting one full question from each module.

Textbooks:

1. Carl Hamacher, Zvonko Vranesic, Safwat Zaky, Computer Organization, 5th Edition, Tata McGraw Hill, 2002. (Listed topics only from Chapters 1, 2, 4, 5, 6, 7, 8, 9 and 12)

Reference Books:

1. William Stallings: Computer Organization & Architecture, 9th Edition, Pearson, 2015.

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