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Future Vision

By K B Hemanth Raj

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Sixth Semester B.E. Degree Examination, Dec.2018/Jan. 2019

VLSI Design

Time: 3 hrs.

Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- 1 a. Mention any two differences between CMOS and Bipolar technology. (02 Marks)
- b. Write all the mask steps of p-well process. (06 Marks)
- c. With neat diagrams, explain the cut off, linear and saturation regions formation in MOSFET with different values of V_{gs} and V_{ds} . (08 Marks)

OR

- 2 a. Explain body effect as non ideal IV effects of MOSFET. (03 Marks)
- b. Explain Noise margin, with respect to CMOS inverter. (05 Marks)
- c. Explain the steps of n-MOS fabrication with neat diagram. (08 Marks)

Module-2

- 3 a. With a neat diagram, explain λ - rules for buried and butting contact and show the cross sectional view of same. (white any one structure buried contact). (08 Marks)
- b. Estimate the rise time and fall time of a CMOS inverter and summarise the result. (08 Marks)

OR

- 4 a. Define sheet resistance, with equation. (02 Marks)
- b. Calculate the area capacitance of the layer below [Refer Fig.Q4(b)] :



Fig.Q4(b)

- i) If the layer is metal – 1 and relative capacitance value is $0.075 \square C_g$
- ii) if the layer is polysilicon and relative capacitance value is $0.1 \square C_g$. (06 Marks)
- c. Write the schematic and stick diagram for Boolean expression $y = (a + bc)$. (implement using CMOS logic). (08 Marks)

Module-3

- 5 a. Design a 4bit, 4×4 barrel shifter. Write the nMOS implementation and strategy for the same. (08 Marks)
- b. Explain carry select adder with neat block diagram. (08 Marks)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

OR

- 6 a. Define regularity. (02 Marks)
b. Derive the scaling factor for the device parameter :
i) Parasitic capacitance
ii) Channel resistance (06 Marks)
iii) Gate delay.
c. Implement the ALU functions like EX-OR, EX-NOR AND and OR operations with an adder. Write the block diagram of 4-bit ALU using adder element. (08 Marks)

Module-4

- 7 a. Explain the following logics :
i) Clocked CMOS logic (08 Marks)
ii) n-p CMOS logic.
b. Explain parity generator, with the nMOS implementation of parity generator with stick diagram. (08 Marks)

OR

- 8 a. Explain Pseudo-nMOS logic. Find Z_{pu}/Z_{pd} when $V_{inr} = 0.5V_{DD}$, $V_{in} = |V_{tp}| = 0.2V_{DD}$, $V_{DD} = 5V$ and $\mu_n = 2.5\mu p$. (08 Marks)
b. Explain the 4-way data selector (multiplexer) with Boolean equation and nMOS based stick diagram. (08 Marks)

Module-5

- 9 a. Write the system timing considerations. (08 Marks)
b. Explain logic verification principle. (08 Marks)

OR

- 10 a. Explain three transistor dynamic RAM with neat circuit and stick diagram. (06 Marks)
b. What are design manufacturability. (10 Marks)

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