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By K B Hemanth Raj

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15EC63

Sixth Semester B.E. Degree Examination, June/July 2018
VLSI Design

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing one full question from each module.

Module-1

1 a. Discuss the working of nMOS enhancement mode transistor operation with neat diagrams. **(06 Marks)**

b. Explain the CMOS inverter DC characteristics highlighting the regions of operation. **(10 Marks)**

OR

2 a. With neat diagrams discuss the nMOS fabrication process steps. **(09 Marks)**

b. Explain the following :
(i) Channel length modulation
(ii) Noise Margin **(07 Marks)**

Module-2

3 a. Discuss the CMOS design style with a diagram. **(05 Marks)**

b. Draw the stick diagram for the following using CMOS logic:
(i) $Y = \overline{A + B + C}$ (ii) 2 i/p NAND gate **(05 Marks)**

c. Discuss the different contact cuts with an example to each. **(06 Marks)**

OR

4 a. With a diagram derive an expression for sheet resistance and mention the R_s values of metal, p and n transistor channels for 5 µm technology. **(05 Marks)**

b. Derive an equation for rise time and fall time with respect to CMOS inverter. **(08 Marks)**

c. Draw the circuit and stick diagram for 2 i/p NOR gate using CMOS logic. **(03 Marks)**

Module-3

5 a. Explain the constant field, constant voltage scaling models with a diagram and scaling effect table. **(06 Marks)**

b. Discuss the problems associated in VLSI design. How do you reduce them? **(05 Marks)**

c. Discuss the different bus architectures. **(05 Marks)**

OR

6 a. Discuss the design of a 4-bit adder. **(07 Marks)**

b. With relevant diagram discuss Manchester carry chain operation. **(05 Marks)**

c. Explain the carry select adder with a diagram. **(04 Marks)**

Module-4

7 a. Discuss the programmable logic array with its structure and floor plan. **(05 Marks)**

b. Discuss the architectural issues related to VLSI sub system design. **(06 Marks)**

c. Discuss the design of Data selectors. **(05 Marks)**

OR

8 a. Explain the architecture of field programmable gate array. **(10 Marks)**

b. Discuss the FPGA abstractions with a diagram. **(06 Marks)**

Module-5

9 a. Explain three transistor DRAM with its diagram and stick diagram. **(07 Marks)**

b. Discuss the ASM chart for JK flip flop with its NAND logic arrangement. **(09 Marks)**

OR

10 a. Explain logic verification process with its functional equivalence diagram. **(06 Marks)**

b. Discuss the design for manufacturability. **(06 Marks)**

c. Discuss the Ad-hoc testing. **(04 Marks)**

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