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VLSI DESIGN

B.E., VI Semester, Electronics & Communication Engineering

[As per Choice Based Credit System (CBCS) Scheme]

Course Code	**17EC63**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**04**	**SEE Marks**	**60**
Total Number of Lecture Hours	**50 (10 Hours / Module)**	**Exam Hours**	**03**

CREDITS – 04

Course Objectives: The objectives of the course is to enable students to:

- Impart knowledge of MOS transistor theory and CMOS technologies
- Impart knowledge on architectural choices and performance tradeoffs involved in designing and realizing the circuits in CMOS technology
- Cultivate the concepts of subsystem design processes
- Demonstrate the concepts of CMOS testing

Module-1

Introduction: A Brief History, MOS Transistors, MOS Transistor Theory, Ideal I-V Characteristics, Non-ideal I-V Effects, DC Transfer Characteristics (1.1, 1.3, 2.1, 2.2, 2.4, 2.5 of TEXT2).

Fabrication: nMOS Fabrication, CMOS Fabrication [P-well process, N-well process, Twin tub process], BiCMOS Technology (1.7, 1.8,1.10 of TEXT1). **L1, L2**

Module-2

MOS and BiCMOS Circuit Design Processes: MOS Layers, Stick Diagrams, Design Rules and Layout.

Basic Circuit Concepts: Sheet Resistance, Area Capacitances of Layers, Standard Unit of Capacitance, Some Area Capacitance Calculations, Delay Unit, Inverter Delays, Driving Large Capacitive Loads (3.1 to 3.3, 4.1, 4.3 to 4.8 of TEXT1).

L1, L2, L3

Module-3

Scaling of MOS Circuits: Scaling Models & Scaling Factors for Device Parameters

Subsystem Design Processes: Some General considerations, An illustration of Design Processes, **Illustration of the Design Processes**- Regularity, Design of an ALU Subsystem, The Manchester Carry-chain and Adder Enhancement Techniques(5.1, 5.2, 7.1, 7.2, 8.2, 8.3, 8.4.1, 8.4.2 of TEXT1). **L1, L2, L3**

Module-4

Subsystem Design: Some Architectural Issues, Switch Logic, Gate(restoring) Logic, Parity Generators, Multiplexers, The Programmable Logic Array (PLA) (6.1to 6.3, 6.4.1, 6.4.3, 6.4.6 of TEXT1).

FPGA Based Systems: Introduction, Basic concepts, Digital design and FPGA's, FPGA based System design, FPGA architecture, Physical design for FPGA's (1.1 to 1.4, 3.2, 4.8 of TEXT3). **L1, L2, L3**

Module-5

Memory, Registers and Aspects of system Timing- System Timing Considerations, Some commonly used Storage/Memory elements (9.1, 9.2 of TEXT1).

Testing and Verification: Introduction, Logic Verification, Logic Verification Principles, Manufacturing Test Principles, Design for testability (12.1, 12.1.1, 12.3, 12.5, 12.6 of TEXT 2). **L1, L2, L3**

Course outcomes: At the end of the course, the students will be able to:

- Demonstrate understanding of MOS transistor theory, CMOS fabrication flow and technology scaling.
- Draw the basic gates using the stick and layout diagrams with the knowledge of physical design aspects.
- Interpret Memory elements along with timing considerations
- Demonstrate knowledge of FPGA based system design
- Interpret testing and testability issues in VLSI Design
- Analyze CMOS subsystems and architectural issues with the design constraints.

Text Books:

1. **"Basic VLSI Design"**- Douglas A. Pucknell& Kamran Eshraghian, PHI 3rd Edition (original Edition – 1994).
2. **"CMOS VLSI Design- A Circuits and Systems Perspective"-** Neil H.E. Weste, David Harris, Ayan Banerjee, 3rd Edition, Pearson Education.
3. **"FPGA Based System Design"-** Wayne Wolf, Pearson Education, 2004, Technology and Engineering.